```
;PALASM Design Description

;------------------------ Declaration Segment ------------------------

TITLE     CPU11 - Convergence Circuit Address Decoder
PATTERN   U81 of Control Board
REVISION  1.1
AUTHOR    Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      May 3, 1992

CHIP   CPU   PALCE16V8

;------------------------ Descriptions ------------------------------
;
; This IC allows access by the 68000 to the convergence circuit RAM
; (U46, U65, and U75) and the "Zone" latch (U40). Chip select CS_WAVE
; (CS-WAVE*) from U28 is strobed low for accesses in the address range
; E0000-EFFFE. This address range is decoded as follows:
;
;      E0000 - E0FFE     Red RAM (U46)
;      E1000 - E1FFE     Green RAM (U65)
;      E2000 - E2FFE     Blue RAM (U75)
;      E3000 - E3FFE     Zone latch (U40)
;
; The PAL outputs write enable signals for the three RAMs and the latch,
; as well as direction signals for the RAM tranceivers (U49, U61, U71).
; The register (U40) is write-only.
;
; Revision History:
;
;   V1.0 - original
;   V1.1 - clean-up of equation syntax in design file - no actual
;          change to content of JEDEC file
;
;------------------------ PIN Declarations --------------------------

PIN   1    CLK           COMBINATORIAL ; INPUT  N/C
PIN   2    CS_WAVE       COMBINATORIAL ; INPUT  convergence chip select
PIN   3    RW            COMBINATORIAL ; INPUT  CPU read/write signal
PIN   4    WU            COMBINATORIAL ; INPUT  CPU UDS* gated by R/W
PIN   5    I4            COMBINATORIAL ; INPUT  N/C
PIN   6    A12           COMBINATORIAL ; INPUT  CPU address bit
PIN   7    A13           COMBINATORIAL ; INPUT  CPU address bit
PIN   8    A14           COMBINATORIAL ; INPUT  CPU address bit
PIN   9    I8            COMBINATORIAL ; INPUT  N/C
PIN   10   GND
PIN   11   OE            COMBINATORIAL ; INPUT  output enable (test only)
PIN   12   IO0           COMBINATORIAL ; OUTPUT N/C
PIN   13   R_WE          COMBINATORIAL ; OUTPUT write enable for U46
PIN   14   G_WE          COMBINATORIAL ; OUTPUT write enable for U65
PIN   15   B_WE          COMBINATORIAL ; OUTPUT write enable for U75
PIN   16   WR_NLATCH     COMBINATORIAL ; OUTPUT write enable for U40
PIN   17   GATE_R        COMBINATORIAL ; OUTPUT U49 xcvr direction
PIN   18   GATE_G        COMBINATORIAL ; OUTPUT U61 xcvr direction
PIN   19   GATE_B        COMBINATORIAL ; OUTPUT U71 xcvr direction
PIN   20   VCC
```